

U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.256US0	10/052,924
	Applicant(s)	
(Use several sheets if necessary)	Mokhlesi et al.	
	Filing Date	Group
	January 18, 2002	2818

## U.S. Patent Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
HU	1	4,630,086	12/16/86	Sato et al.		
	2	5,172,338	12/15/92	Mehrotra et al.		
	3	5,172,338	7/8/97	Mehrotra et al.		
	4	5,418,752	5/23/95	Harari et al.		
	5	5,712,180	1/27/98	Guterman et al.		
	6	5,768,192	6/16/98	Eitan		
	7	5,892,706	4/6/99	Shimizu et al.		
	8	6,044,109	3/28/00	Cernea et al.		
	9	6,103,573	8/15/00	Harari et al.		
HU	10	6,222,762	4/24/01	Guterman et al.		

## U.S. Published Patent Application Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

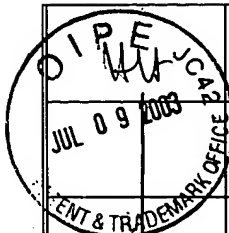
## Foreign Patent Documents

							Translation	
	Document	Date	Country	Class	Subclass		Yes	No

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

HU	11	Bauza et al., "In-Depth Exploration of Si-SiO <sub>2</sub> Interface Traps in MOS Transistors Using the Charge Pumping Technique," <i>IEEE Transactions on Electron Devices</i> , Vol. 44, No. 12, December 1997, pp. 2262-2266.
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	14	Hung et al., "Random Telegraph Noise of Deep-Submicrometer MOSFET's," <i>IEEE Electron Device Letters</i> , Vol. 11, No. 2, February 1990, pp. 90-92.
HU	15	Hung et al., "A Unified Model for the Flicker Noise in Metal-Oxide-Semiconductor Field-Effect Transistors," <i>IEEE Transactions on Electron Devices</i> , Vol. 37, No. 3, March 1990, pp. 654-665.

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	16	Fleetwood et al., "Effects of Oxide Traps, Interface Traps, and Border Traps on Metal-Oxide-Semiconductor Devices," <i>J. Appl. Phys.</i> , Vol. 73, No. 10, 15, May 1993, pp. 5058-5075.
	17	Iafrate et al., "Capacitive Nature of Atomic-Sized Structures," <i>Physical Review B</i> , Vol. 52, Number 15, October 15, 1995-I, pp. 10-737 - 10-739.
	18	Jallepalli et al., "Electron and Hole Quantization and Their Impact on Deep Submicron Silicon p- and n-MOSFET Characteristics," <i>IEEE Transactions on Electron Devices</i> , Vol. 44, No. 2, February 1997, pp. 297-303.
	19	Klumperink et al., "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 35, No. 7, July 2000, pp. 994-1001.
	20	Korotkov, "Intrinsic Noise of the Single-Electron Transistor," <i>Physical Review B</i> , Vol. 49, No. 15, April 15, 1994, pp. 10 381 - 10 392.
	21	Kumar et al., "1/f Noise Model of Fully Overlapped Lightly Doped Drain MOSFET," <i>IEEE Transactions on Electron Devices</i> , Vol. 47, No. 7, July 2000, pp. 1426 - 1430.
	22	Ma et al., "New Insight into High-Field Mobility Enhancement of Nitrided-Oxide N-MOSFET's Based on Noise Measurement," <i>IEEE Transactions on Electron Devices</i> , Vol. 41, No. 11, November 1994, pp. 2205 - 2209.
	23	Mokhlesi et al., "A Solution for Current-Voltage Characteristics of Multiple Coupled Mesoscopic Tunnel Junctions," <i>Superlattices and Microstructures</i> , Vol. 21, No. 1, 1997, pp. 15-19.
	24	Nemirovsky et al., "1/f Noise in CMOS Transistors for Analog Application," <i>IEEE Transaction on Electron Devices</i> , Vol. 48, No. 5, May 2001, pp. 921-927.
	25	Ohjuro et al., "An Epitaxial Channel MOSFET for Improving Flicker Noise Under Low Supply Voltage," <i>2000 Symposium on VLSI Technology Digest of Technical Papers</i> , pp. 160-161.
	26	Pacelli et al., "Quantum Effects on the Extraction of MOS Oxide Traps by 1/f Noise Measurements," <i>IEEE Transactions on Electron Devices</i> , Vol. 46, No. 5, May 1999, pp. 1029-1035.
	27	Pohm, A.V., et al., "The Design of a One Megabit Non-Volatile M-R Memory Chip Using 1.5*5 mu m Cells," <i>IEEE Transactions on Magnetics</i> , Vol. 24, No. 6, November 1988, pp. 3117-3119.
	28	Surya et al., "Effects of Low-Energy Back Surface Gettering on the Properties of 1/f Noise in n-Channel Nitrided MOSFETs," <i>ICSE '96 Proc.</i> , Nov. 1996, Penang, Malaysia, pp. 59-62
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11/1	30	van der Wel et al., "MOSFET 1/f Noise Measurement Under Switched Bias Conditions," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 1, January 2000, pp. 43-46.

Examiner

Huan Hoang

Date Considered

8/7/03

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.